WHAT IS CLAIMED IS:

1. A method of forming a semiconductor device, comprising the steps of:

forming dummy vias in a semiconductor wafer between a main die area and a saw lane of the semiconductor wafer; and

sawing the semiconductor wafer along the saw lane to separate the main die area from the semiconductor wafer.

2. The method of claim 1, wherein the semiconductor wafer includes a plurality of metal layers and a dielectric layer between at least two of the metal layers, the step of forming dummy vias including forming the dummy vias in the dielectric layer.

3. The method of claim 2, wherein the dielectric layer comprises a low k dielectric material.

4. The method of claim 3, further comprising forming a scribe line monitor area on the semiconductor wafer, the saw lane and the dummy vias being located within the scribe line monitor area.

5. The method of claim 4, wherein the metal layers have non-functional metal tiles in the scribe line monitor area, with at least one of the dummy vias being formed between and contacting metal tiles in two of the metal layers.

6. The method of claim 5, wherein the dummy vias consist of metal.

7. The method of claim 6, wherein the step of forming dummy vias includes manual laying out of the dummy vias within the scribe line monitor area.

8. The method of claim 6, wherein the step of forming dummy vias includes automated placing of the dummy vias within the scribe line monitor area.

9. A semiconductor device comprising:
a main die area containing functional circuitry;
a scribe line monitor area circumferentially surrounding the main die area; and
stress relief elements in the scribe line monitor area.

10. The semiconductor device of claim 9, wherein the stress relief elements include dummy vias in the scribe line monitor area.

11. The semiconductor device of claim 10, wherein the scribe line monitor area includes at least a first metal layer, a dielectric layer on the first metal layer, and a second metal layer on the first dielectric layer.

12. The semiconductor device of claim 11, wherein the dielectric layer is a low k dielectric layer.

13. The semiconductor device of claim 12, wherein the first and second metal layers contain non-functional metal tiles.

14. The semiconductor device of claim 13, wherein at least one of the dummy vias is connected between one of the metal tiles in the first metal layer and one of the metal tiles in the second metal layer.

15. The semiconductor device of claim 14, wherein the scribe line monitor area includes a saw lane, the dummy vias being located between the saw lane and the main die area.

16. A semiconductor arrangement comprising:

a main die area;

a surrounding area circumferentially surrounding the main die area; and

crack stop elements in the surrounding area.

17. The semiconductor arrangement of claim 16, wherein the crack stop elements include dummy vias.

18. The semiconductor arrangement of claim 17, wherein the surrounding area is a scribe line monitor area.

19. The semiconductor arrangement of claim 18, wherein the scribe line monitor area includes a first metal layer, a dielectric area on the dielectric layer, and a second metal layer on the dielectric layer, each of the first and second metal layers including non-functional metal tiles, and at least some of the dummy vias being connected between the metal tiles of the first and second metal layers.

20. The semiconductor arrangement of claim 19, wherein the dielectric layer comprises a low k dielectric material.